REMARKS

Claims 1-5, 9-19, 21 and 22 remain pending in this application. Claim 18 has been amended by this response. The amendments have been made to clarify the claimed subject matter. Support for the claim amendments is found throughout the specification and specifically at page 7, lines 1-19. No new matter has been added by these amendments.

Rejection of claims 18 and 19 under 35 U.S.C. 101

Claims 18 and 19 are rejected under 35 U.S.C. 101 as not positively reciting any structure within the body of the claim which ties the claim to a statutory category and that the structure needs to link the inventive concept of the application to a statutory category. Claim 18 has been amended to recite "the signal containing an image representative data stream containing data packets received by a digital television receiver" to specifically tie the method to a machine conditioned for operating in the claimed manner. Moreover, the claimed arrangement sets forth specific hardware elements tied to the claimed steps. A digital television receiver is any device able to receive digital television signals. In the claimed method, within the Digital television receiver a signal is demodulated, errors in the demodulated signal are detected to produce a first error signal, and the first error signal is forwarded to a transport processor. A synchronization signal is also forwarded to a transport processor to associate the first error signal with a particular data packet. A second error signal is generated in response to the synchronization signal. Each discrete second error signal frame is started and stopped before and after an associated data packet. The system includes specific processors that are specifically conditioned to operate to implement the claimed features. Thus, the steps of demodulating, error detecting, forwarding, and generating are performed by the digital television receiver. Furthermore, the operations recited in the claims change and process underlying data, which cannot be performed mentally, verbally or without a machine. Specifically, it is respectfully submitted that, contrary to the assertion of the Office Action, demodulation of a signal containing an image representative data stream cannot be demodulated mentally, verbally or without a machine. Therefore, Applicant respectfully submits that the claimed system satisfied both prongs of the machine or transformation test set forth in *In re Bilski*. Consequently, withdrawal of the rejection of claim 18 is respectfully requested. As claim 19 is dependent on claim 18, withdrawal of claim 19 is also respectfully requested.

Rejection of claims 1-5, 9-19 and 21-22 under 35 U.S.C. 103(a)

Claims 1-5, 9-19 and 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashita (5,506,903) and Boyce (6,317,462) in view of Komatsu (6,097,879).

The present claimed arrangement provides an apparatus for processing a received signal containing a datastream. A signal decoder generates a first error signal in response to indecipherable data received by the decoder. A transport processor receives the first error signal and generates a second error signal after receiving the first error signal. The second error signal begins at an earlier time than an associated data packet and the second error signal ends at a later time than the associated data packet.

Yamashita describes a digital multiplex transmission system where a multiplex frame is constructed such that the redundancy of an error correction code can be changed and the information rate principally of digital video data can be changed when the redundancy is changed so that the transmission rate may be fixed. (See col. 2, lines 14-19)

Yamashita, as acknowledged by the Office Action, neither discloses nor suggests "the transport processor generating a second error signal after receiving the first error signal" as recited in claim 1 of the present arrangement. Yamashita only describes errors in frames corrected by a Reed-Solomon decoder using a Reed-Solomon decoder added on the transmission side. However, the Office Action asserts that Boyce describes "the transport processor generating a second error signal after receiving the first error signal" as recited in claim 1 of the present arrangement.

Boyce describes a system that performs Systematic Forward/Error Correction coding on data in a high priority partition. An inter-frame coded video signal, such as an MPEG video signal, employs a data splitting function to split a video stream into a high priority and a low priority partition. The Forward/Error Erasure Corrected high priority partition data and the non-Forward Error/Erasure Corrected low priority partition data are then combined into packets and transmitted over the same network to a receiver, where they are decoded.

Depending on the degree of protection against errors or erasures offered by the particular FEC code that is used, the loss of one or more packets containing high priority data can be corrected with no loss of data in the high priority partition. The effect of the loss of the low partition data in the lost packet or packets, which low partition is not protected, has much less of a deleterious effect on the quality of the decoded signal than would the loss of data from the high priority partition data. By limiting the application of the Forward Error/Erasure Correction to the higher priority partition data, thus protecting against loss of "more important data," the overhead requirement for protection against a given packet loss is reduced. (See col. 3, lines 38-61)

The Office Action further acknowledges that neither Yamashita nor Boyce disclose or suggest "wherein the second error signal begins at an earlier time than an associated data packet, and wherein the second error signal ends at a later time than the associated data packet" as recited in claim 1 of the present arrangement. Both Yamashita and Boyce only describe the use of Reed-Solomon decoders to generate error signals in response to indecipherable data to produce a high quality image while allowing for minimal packet loss and low delay times. However, the Office Action asserts that Komatsu describes the aforementioned feature. Applicant respectfully disagrees.

Komatsu describes a video camera apparatus for recording a signal in a digital recording system that can receive external analog standard video and audio signals from TV broadcasting or analog video decks. Signals can be converted into digital signals and compressed. Data can be recorded within the video camera. (See col. 1, lines 22-27)

Komatsu, like Yamashita and Boyce, neither discloses nor suggests that "the second error signal begins at an earlier time than an associated data packet, and...the second error signal ends at a later time than the associated data packet" as recited in claim 1 of the present arrangement. The present claimed arrangement provides a packet error signal generator that advantageously provides an error signal that has a duration greater than its associated data packet and begins before and ends after the associated data packet to result in the error signal bracketing the underlying data packet (page 5, lines 4-8). This allows for "microprocessor 60" to receive "the packet error signal at least one segment prior to the time that the packet

error signal must be used" in order to "accommodate system clock rate variations (page 8, lines 10-19). While Komatsu describes a phase error detecting circuit, the operation of the circuit is not analogous to that of the present claimed arrangement. Applicant further asserts that the Office Action has misinterpreted Komatsu. The Office Action asserts Fig. 12 of Komatsu shows that, after time t, section d shows that phase error is at a logical high, and after time t, in section b, when the clock starts at logical low, the signal of section d is already at logical high. (See col. 15, lines 28-58). However, the clock of Komatsu is not the same as "an associated data packet" of the received data stream as recited in claim 1 of the present arrangement. Instead, the clock of Komatsu simply represents a pulsed external clock cycle to determine when synchronization signals are held in order to allow a phase error detecting circuit to hold the clock level in order to find a phase difference (col. 15, lines 10-26). In contrast, the present claimed arrangement provides a "second error signal" that begins before and ends after "an associated data packet" to create a bracket for each data packet. Furthermore, Fig. 12 of Komatsu further shows that in section b, when the clock moves from logical high back to logical low, the error signal of section d remains at logical high. However, since the clock of Komatsu is not the same as "an associated data packet" of the present claimed arrangement, the fact that the phase error signal of Komatsu begins earlier and ends later than the clock signal does not result in a "second error signal" that "begins at an earlier time than an associated data packet" and "ends at a later time than the associated data packet." Instead, the sync output represented by section a in Fig. 12 represents the output data, and Fig. 12 shows that section d, which represents the phase error detector, actually starts later in time and ends later in time than section a. Thus, Komatsu, like Yamashita and Boyce, neither discloses nor suggests that "the second error signal begins at an earlier time than an associated data packet, and…the second error signal ends at a later time than the associated data packet" as recited in claim 1 of the present arrangement.

In addition, the combination of Yamashita, Boyce, and Komatsu, similar to the individual systems, also neither discloses nor suggests that "the second error signal begins at an earlier time than an associated data packet, and…the second error signal ends at a later time than the associated data packet" as recited in claim 1 of the present arrangement. A combination of Yamashita, Boyce, and Komatsu results in a system using a Reed-Solomon decoder to correct errors in order to produce a high quality image while minimizing packet

loss and delay. However, the combination would not disclose or suggest that "the second error signal begins at an earlier time...and ends at a later time than the associated data packet." The clock of Komatsu is not "an associated data packet" of the present claimed arrangement. In addition, even if the clock were "an associated data packet," section d of Fig. 12 of Komatsu shows that the phase error detector does not reset to begin at an earlier time than every associated data packet since section d shows the phase error detector remaining in logical high for more than one clock cycle, as shown in section b. Thus, the combination of Yamashita, Boyce, and Komatsu, similar to the individual systems, neither discloses nor suggests that "the second error signal begins at an earlier time than an associated data packet, and...the second error signal ends at a later time than the associated data packet" as recited in claim 1 of the present arrangement. Therefore, it is respectfully submitted that the rejection of claim 1 is satisfied and should be withdrawn.

Dependent claims 2-5, 9 and 10 are dependent on claim 1 and are considered patentable for the reasons set forth above regarding claim 1. Therefore, it is respectfully submitted that the rejection of claims 2-5, 9 and 10 is satisfied and should be withdrawn.

Independent claim 11 contains features similar to those found in claim 1 and is considered patentable for the reasons set forth above regarding claim 1. Therefore, it is respectfully submitted that the rejection of claim 11 is satisfied and should be withdrawn.

Dependent claims 12-17 are dependent on claim 11 and are considered patentable for the reasons set forth above with regard to claim 11. Therefore, it is respectfully submitted that the rejection of claims 12-17 is satisfied and should be withdrawn.

Independent claim 18 provides a method claim containing features similar to those found in claims 1 and 11 and is considered patentable for the reasons set forth above with regard to claims 1 and 11. Therefore, it is respectfully submitted that the rejection of claim 18 is satisfied and should be withdrawn.

Dependent claims 19 and 21 are dependent on claim 18 and are considered patentable for the reasons set forth above regarding claim 18. Therefore, it is respectfully submitted that the rejection of claims 19 and 21 is satisfied and should be withdrawn.

Independent claim 22 contains features similar to those found in claims 1 and 11 and is considered patentable for the reasons set forth above with regard to claims 1 and 11. Therefore, it is respectfully submitted that the rejection of claim 22 is satisfied and should be withdrawn.

In view of the above remarks and amendments to the claims it is respectfully submitted that this rejection is satisfied and should be withdrawn.

Having fully addressed the Examiner's rejections, it is believed that, in view of the preceding amendments and remarks, this application stands in condition for allowance. Accordingly then, reconsideration and allowance are respectfully solicited. If, however, the Examiner is of the opinion that such action cannot be taken, the Examiner is invited to contact the applicant's attorney at the phone number below, so that a mutually convenient date and time for a telephonic interview may be scheduled.

No additional fee is believed due. However, if an additional fee is due, please charge the additional fee to Deposit Account 07-0832.

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